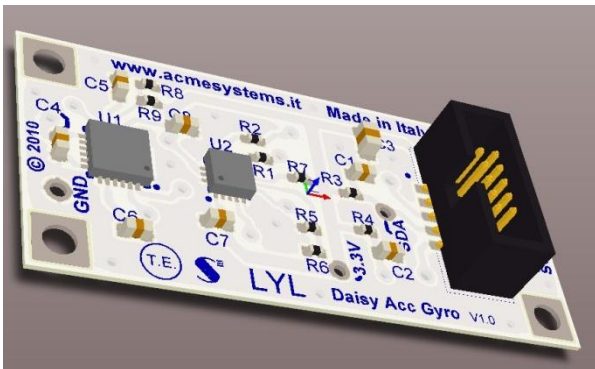


DAISY-7 6DOF DIGITAL MEMS ACCELEROMETER AND GIROSCOPE



Features

- Digital triple axis accelerometer and digital triple axis gyros
- Digital-output X, Y, and Z-Axis $\pm 2g/\pm 4g/\pm 8g$ dynamically selectable full-scale acceleration
- Digital-output X, Y, and Z-Axis angular rate sensors (gyros) on one integrated circuit with a sensitivity of 14.375 LSBs per $^{\circ}/\text{sec}$ and a full-scale range of $\pm 2000^{\circ}/\text{sec}$
- Fast Mode I²C (400kHz) serial interface
- 16 bit data output ADCs provide simultaneous sampling of gyros and acceleration while requiring no external multiplexer
- Daisy Ready
- 3 independent programmable interrupt generators for free-fall and motion detection
- Sleep to wake-up function
- Embedded self-test
- 10000 g high shock survivability
- Enhanced bias and sensitivity temperature stability reduces the need for user calibration
- ECOPACK[®] RoHS and "Green" compliant

Applications

- Motion activated functions
- Free-fall detection
- Intelligent power saving for handheld devices
- Appliances and robotics
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation
- navigation systems
- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- IMU inertial measurement unit

Sommario

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1.0 Sensor Specifications

Parameter	Test Conditions	Min.	Typ.	Max	Unit
ACCELEROMETER LIS331DLH					
Mes.Range	FS bit set to 00		±2.0		g
	FS bit set to 01		±4.0		
	FS bit set to 11		±8.0		
Sensitivity	FS bit is set to 00	0.9	1	1.1	mg/digit
	FS bit is set to 01	1.8	2	2.2	
	FS bit is set to 11	3.5	3.9	4.3	
sensitivity change vs temperature			±0.01		%/°C
Typical zero-g level offset accuracy			±20		mg
Zero-g level change v.s temperature			±0.1		mg/°C
Noise density			218		µg/√Hz
Output Data Rate	DR bit set to 00		50		Hz
	DR bit set to 01		100		
	DR bit set to 10		400		
	DR bit set to 11		1000		
Gyro ITG-3200					
Full Scale Range			±2000		°/S
Gyro ADC Word Length			16		bit
Sensitivity Scale Factor			14.375		LSB/(°/S)
Sensitivity Scale factor tolerance		+6		-6	%
Sensitivity Scale Factor Variation Over			±10		%
Nonlinearity			0.2		%
Cross-Axis sensitivity			2		%
Initial Zero Tolerance			±40		°/S
Linear Acceleration Sensitivity			0.1		°/S/g
RMS Noise			0.38		°/S-rms
Rate Noise Spectral Density			0.03		°/S/√Hz
Output Data Rate Max				1000	Hz
Temperature Sensor					
Range		-30		+85	°C
sensitivity			280		LSB/°C

2.0 Default I2C address:

Daisy adapter: D8 for no use interrupt Pin, or D6 , D1 for use Interrupt INT INT1 INT2.

I2C ADDRESS accelerometer LIS331DLH:

AD0 = 0	0011000(DEF)(0x18h)
AD0 = 1	0011000(Alternative)(0x19h)

I2C ADDRESS Giroscope ITG-3200:

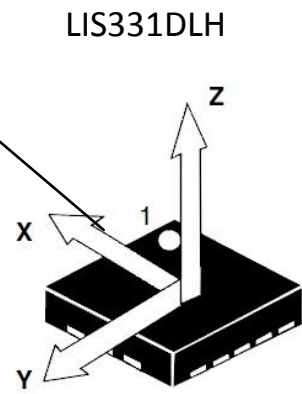
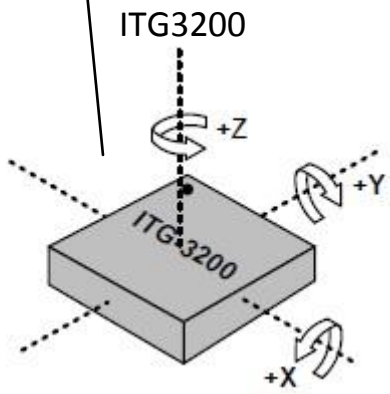
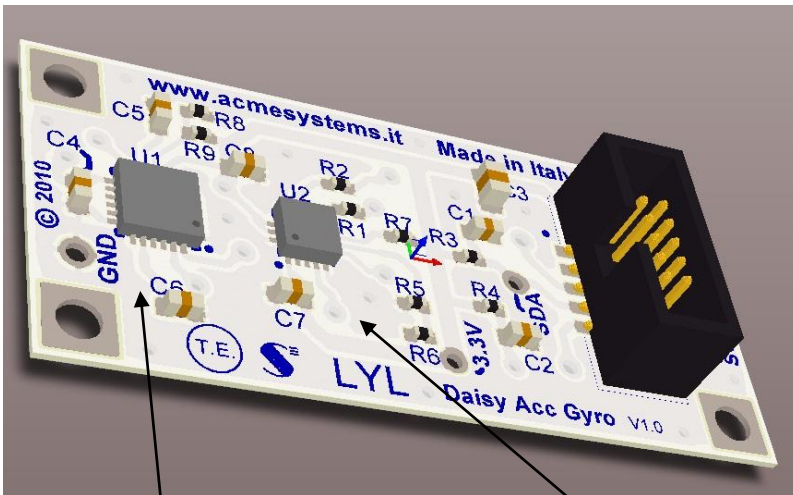
AD0 = 0	1101000 (DEF)(0x68h)
AD0 = 1	1101001(Alternative)(0x69h)

3.0 Pin description and orientation

J1 connector:

Pin1	+3.3V
Pin2	No Connected
Pin3	No Connected
Pin4	INT1 connected to LIS331DLH
Pin5	INT2 connected to LIS331DLH
Pin6	INT connected to ITG-3200
Pin7	I2C-SDA
Pin8	I2C-SCL
Pin9	No Connected
Pin10	GND

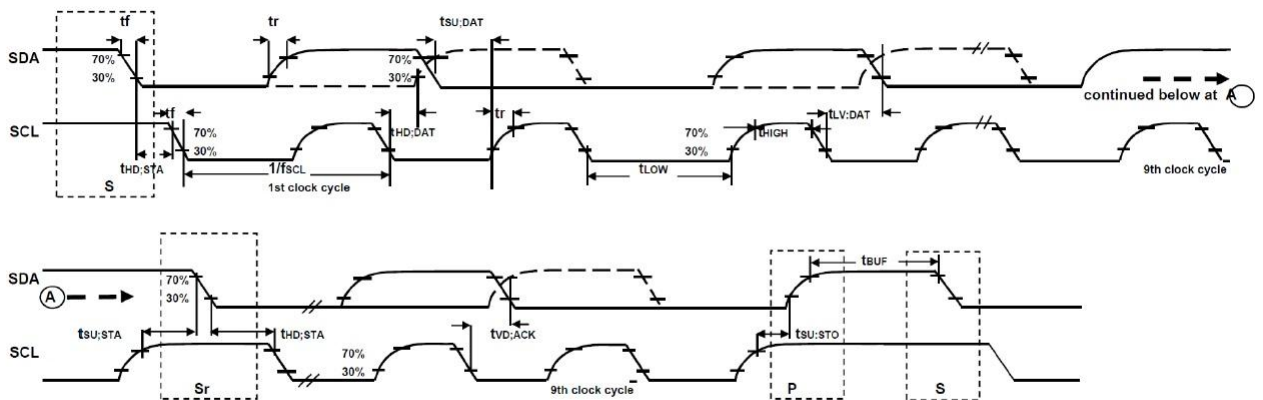
Orientation:



4.0 I²C Timing Characterization

Typical Operating Circuit of Section 4.2, VDD = 3.3V, VLOGIC = 1.8V±5%, 2.5V±5%, 3.0V±5%, or 3.3V±5%, T_A=25°C.

Parameters	Min	Max	Units
f _{SCL} , SCL Clock Frequency	0	400	KHz
t _{HDSDA} , START condirion Hold Time	0.6		us
t _{LOW} , SCL Low Period	1.3		us
t _{SUSTA} , Repeated START Condition Setup Time	0.6		us
t _{HDDAT} , SDA Data Hold Time	0		us
t _{SUDAT} , SDA Data Setup Time	100		ns
T _r , SDA and SCL Rise Time	20	300	ns
T _f , SDA and SCL Fall Time	20	300	ns
t _{SUSTO} , STOP Condition Setup Time	0.6		us
t _{BUS} , Buss Free Time	1.3		us
t _{VDDAT} , Data Valid Time		0.9	us
t _{VDAck} , Data Valid Acknowledge Time		0.9	us



I²C Bus Timing Diagram

5.0 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Maxium Value	Unit
Vdd	Supply voltage	-0.3 to 6	V
Vin	Input voltage	-0.3 to 6	V
A _{POW}	Acceleration	3000 g for 0.5ms 10000 g for 0.1ms	
T _{OP}	Operating Temperature Range	-40 to +85	
T _{STG}	Storage Temperature range	-40 to +125	
ESD	Eletrostatic discharge protection	4(HBM)	KV
		1.5(CDM)	KV
		200(MM)	V

Supply voltage on any pin should never exceed 6.0 V

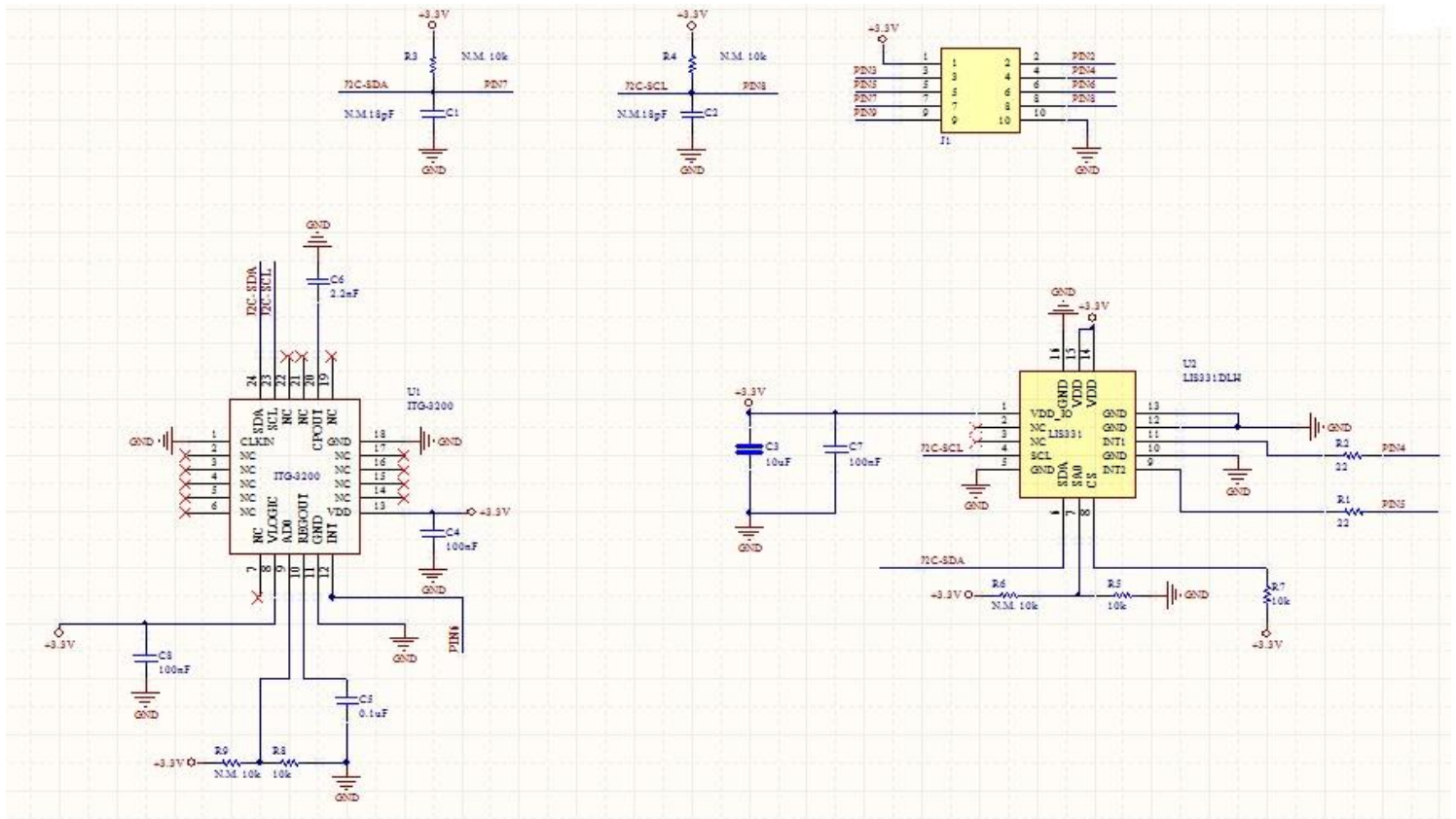


This is a mechanical shock sensitive device, improper handling can cause permanent damages to the part



This is an ESD sensitive device, improper handling can cause permanent damages to the part

6.0 Scheme



7.0 Digital interfaces I2C

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave Address (SAD) associated to the LIS331DLH is 001100xb. **SDO/SA0** pad can be used to modify less significant bit of the device address. If SA0 pad is connected to voltage supply, LSB is '1' (address 0011001b, disconnect R5 and solder R6) else if SA0 pad is connected to ground, LSB value is '0' (address 0011000b default assemble configuration). This solution permits to connect and address two different accelerometers to the same I2C lines.

The slave address of the ITG-3200 devices is b110100X which is 7 bits long. The LSB bit of the 7 bit address is determined by the logic level. This allows two ITG-3200 devices to be connected to the same I2C bus. When used in this configuration, the address of the one of the devices should be b1101000 (default assemble configuration) and the address of the other should be b1101001 (disconnect R8 and solder R9). The I2C address is stored in register 0 (WHO_AM_I register).

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I2C embedded inside the LIS331DLH behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the Master will transmit to the slave with direction unchanged. Table explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

SAD+Read/Write patterns LIS331DLH

Command	SAD[6:1]	SAD[0]=SA0	R/W	SAD+RW
Read	001100	0	1	00110001 (31h)
Write	001100	0	0	00110000 (30h)
Read	001100	1	1	00110011 (33h)
Write	001100	1	0	00110010 (32h)

SAD+Read/Write patterns ITG-3200

Command	SAD[6:1]	SAD[0]=SA0	R/W	SAD+RW
Read	110100	0	1	11010001 (D1h)
Write	110100	0	0	11010000 (D0h)
Read	110100	1	1	11010011 (D3h)
Write	110100	1	0	11010010 (D2h)

Transfer when master is writing one byte to slave

Master	ST	SAD+W		SUB		DATA		SP
Slave			SAK		SAK		SACK	

Transfer when master is writing multiple bytes to slave:

Master	ST	SAD+W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SACK		SAK	

Transfer when master is receiving (reading) one byte of data from slave:

Master	ST	SAD+W		SUB		SR	SAD+R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the subaddress field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read. In the presented communication format MAK is Master acknowledge and NMAK is no master acknowledge.

8.0 Register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

8.1 register LIS331DLH

Name	Type	Address (HEX)	Default
Reserved		00-0E	
WHO_AM_I	R	0F	00110010
Reserved		10-1F	
CTRL_REG1	RW	20	00000111
CTRL_REG2	RW	21	00000000
CTRL_REG3	RW	22	00000000
CTRL_REG4	RW	23	00000000
CTRL_REG5	RW	24	00000000
HP_FILTER_RESET	R	25	
REFERENCE	RW	26	00000000
STATUS_REG	R	27	00000000
OUT_X_L	R	28	Output
OUT_X_H	R	29	Output
OUT_Y_L	R	2A	Output
OUT_Y_H	R	2B	Output
OUT_Z_L	R	2C	Output
OUT_Z_H	R	2D	output
Reserved		2E-2F	
INT1_CFG	RW	30	00000000
INT1_SOURCE	R	31	00000000
INT1_THS	RW	32	00000000
INT1_DURATION	RW	33	00000000
INT2_CFG	RW	34	00000000
INT2_SOURCE	R	35	00000000
INT2_THS	RW	36	00000000
INT2_DURATION	RW	37	00000000
Reserved		38-3F	

8.2 register ITG-3200

Addr Hex	Addr Decimal	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	WHO_AM_I	R/W	-	ID						-
15	21	SMPLRT_DIV	R/W	SMPLRT_DIV							
16	22	DLPF_FS	R/W	-	-	-	FS_SEL			DLPF_CFG	
17	23	INT_CFG	R/W	ACTL	OPEN	LATCH _ INT_EN	INT_ ANYRD_ 2CLEAR	-	ITG_RDY _EN	-	RAW_ RDY_ EN
1A	26	INT_STATUS	R	-	-	-	-	-	ITG_RDY	-	RAW_ DATA_ RDY
1B	27	TEMP_OUT_H	R	TEMP_OUT_H							
1C	28	TEMP_OUT_L	R	TEMP_OUT_L							
1D	29	GYRO_XOUT_H	R	GYRO_XOUT_H							
1E	30	GYRO_XOUT_L	R	GYRO_XOUT_L							
1F	31	GYRO_YOUT_H	R	GYRO_YOUT_H							
20	32	GYRO_YOUT_L	R	GYRO_YOUT_L							
21	33	GYRO_ZOUT_H	R	GYRO_ZOUT_H							
22	34	GYRO_ZOUT_L	R	GYRO_ZOUT_L							
3E	62	PWR_MGM	R/W	H_RESET		SLEEP		STBY_XG	STBY_YG	STBY_ZG	CLK_SEL

9.0 Register description

9.1 register LIS331DLH

WHO_AM_I (0Fh)

0	0	1	1	0	0	1	0
---	---	---	---	---	---	---	---

Device identification register.

This register contains the device identifier that for LIS331DLH is set to 32h.

CTRL_REG1 (20h)

PM2	PM1	PM0	DR1	DR0	ZEN	YEN	XEN
-----	-----	-----	-----	-----	-----	-----	-----

PM2 - PM0	Power mode selection. Default value: 000 (000: Power-down; Others: refer to <i>Table</i>)
DR1, DR0	Data rate selection. Default value: 00 (00:50 Hz; Others: refer to <i>Table</i>)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

PM bits allow to select between power-down and two operating active modes. The device is in power-down mode when PD bits are set to “000” (default value after boot).

shows all the possible power mode configurations and respective output data rates. Output data in the low-power modes are computed with low-pass filter cut-off frequency defined by DR1, DR0 bits.

DR bits, in the normal-mode operation, select the data rate at which acceleration samples are produced. In low-power mode they define the output data resolution. *Table* shows all the possible configuration for DR1 and DR0 bits.

Power mode and low-power output data rate configurations

PM2	PM1	PM0	Power mode selection	Output data rate(HZ)
0	0	0	Power-down	--
0	0	1	Normal mode	ODR
0	1	0	Low-power	0.5
0	1	1	Low-power	1
1	0	0	Low-power	2
1	0	1	Low-power	5
1	1	0	Low-power	10

Normal-mode output data rate configurations and low-pass cut-off frequencies

DR1	DR0	Output Data Rate[Hz] ODR	Low-pass filter cut-off frequency [Hz]
0	0	50	37
0	1	100	74
1	0	400	292
1	1	1000	780

CTRL_REG2 (21h)

BOOT	HPM1	HPM0	FDS	HPen2	HPen1	HPCF1	HPCF0
------	------	------	-----	-------	-------	-------	-------

BOOT	Reboot memory content. Default value:0 (0: normal mode; 1:reboot memory content)
HPM1,HPM0	High pass filter mode selection. Default value: 00 (00: normal mode; other: refer to description continued)
FDS	Filtered data selection. Default value:0 (0: internal filter bypassed;1 data from internal filter sent to output register)
HPen2	High pass filter enabled for interrupt 2 source. Default value: 0 (0: filter bypassed; 1: filter enabled)

CTRL_REG2 description (continued)

HPen1	High pass filter enabled for interrupt 1 source. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPCF1, HPCF0	High pass filter cut-off frequency configuration. Default value: 00 (00: HPc=8; 01: HPc=16; 10: HPc=32; 11: HPc=64)

BOOT bit is used to refresh the content of internal registers stored in the flash memory block. At the device power up the content of the flash memory block is transferred to the internal registers related to trimming functions to permit a good behavior of the device itself.

If for any reason the content of trimming registers was changed it is sufficient to use this bit to restore correct values. When BOOT bit is set to '1' the content of internal flash is copied inside corresponding internal registers and it is used to calibrate the device. These values are factory trimmed and they are different for every accelerometer. They permit a good behavior of the device and normally they have not to be changed. At the end of the boot process the BOOT bit is set again to '0'.

High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode
0	1	Reference signal for filtering
1	0	Normal mode

HPCF[1:0].these bit are used to configure high-pass filter cut-off frequency f_t which is given by:

$$f_t = \ln\left(1 - \frac{1}{HPc}\right) * \frac{f_s}{2\pi}$$

The equation can be simplified to following approximated equation:

$$f_t = \frac{f_s}{6 * HPc}$$

High-pass filter cut-off frequency configuration:

HPcoeff2,1	F_t [Hz] Data rate=50Hz	F_t [Hz] Data rate=100Hz	F_t [Hz] Data rate=400Hz	F_t [Hz] Data rate=1000Hz
00	1	2	8	20
01	0.5	1	4	10
10	0.25	0.5	2	5
11	0.125	0.25	1	2.5

CTRL_REG3 [Interrupt CTRL register] (22h)

IHL	PP_OD	LIR2	I2_CFG1	2_CFG0	LIR1	I1_CFG1	I1_CFG0
-----	-------	------	---------	--------	------	---------	---------

CTRL_REG3 description

IHL	Interrupt active low. Default value:0 (0: active high; 1: active low)
PP_OD	Push-pull/Open drain selection on interrupt pad. Default value 0. (0: push-pull; 1:open drain)
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value 0. (0: interrupt request not latched; 1: interrupt request latched)
I2_CFG1, I2_CFG0	Data signal on INT 2 pad control bits. Default value 00. (see table below)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value 0. (0: interrupt request not latched; 1: interrupt request latched)
I1_CFG1, I1_CFG0	Data signal on INT 1 pad control bits. Default value 00. (see table below)

Data signal on INT 1 and INT 2 pad

I1(2)_CFG1	I1(2)_CFG0	INT 1(2) Pad
0	0	Interrupt 1(2) source
0	1	Interrupt 1 source OR interrupt 2 source
1	0	Data ready
1	1	Boot running

CTRL_REG4 (23h)

BDU	BLE	FS1	FS0	STsign	0	ST	SIM
-----	-----	-----	-----	--------	---	----	-----

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated between MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: data LSB @ lower address; 1: data MSB @ lower address)
FS1, FS0	Full-scale selection. Default value: 00. (00: $\pm 2 g$; 01: $\pm 4 g$; 11: $\pm 8 g$)
STsign	Self-test sign. Default value: 00. (0: self-test plus; 1 self-test minus)
ST	Self-test enable. Default value: 0. (0: self-test disabled; 1: self-test enabled)
SIM	SPI serial interface mode selection. Default value: 0. (0: 4-wire interface; 1: 3-wire interface)

BDU bit is used to inhibit output registers update between the reading of upper and lower register parts. In default mode (BDU = '0') the lower and upper register parts are updated continuously. If it is not sure to read faster than output data rate, it is recommended to set BDU bit to '1'. In this way, after the reading of the lower (upper) register part, the content of that output registers is not updated until the upper (lower) part is read too.

This feature avoids reading LSB and MSB related to different samples.

CTRL_REG5 (24h)

0	0	0	0	0	0	TurnOn1	TurnOn0
---	---	---	---	---	---	---------	---------

TurnOn1, TurnOn0	Turn-on mode selection for sleep to wake function. Default value: 00
---------------------	--

TurnOn bits are used for turning on the **sleep to wake** function.

Sleep to wake configuration:

TurnOn1	TurnOn0	Sleep to wake status
0	0	Sleep to wake function is disabled
1	1	Turned on: The device is in low power mode(ODR is defined in CTRL_REG1)

Setting TurnOn[1:0] bits to 11 the “sleep to wake” function is enabled. When an interrupt event occurs the device is turned to normal mode increasing the ODR to the value defined in CTRL_REG1. Although the device is in normal mode, CTRL_REG1 content is not automatically changed to “normal mode” configuration.

HP_FILTER_RESET (25h)

Dummy register. Reading at this address zeroes instantaneously the content of the internal high pass-filter. If the high pass filter is enabled all three axes are instantaneously set to 0g. This allows to overcome the settling time of the high pass filter.

REFERENCE (26h)

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0
------	------	------	------	------	------	------	------

REFERENCE description

Ref7 - Ref0 Reference value for high-pass filter. Default value: 00h.

This register sets the acceleration value taken as a reference for the high-pass filter output. When filter is turned on (at least one of FDS, HPen2, or HPen1 bit is equal to ‘1’) and HPM bits are set to “01”, filter out is generated taking this value as a reference

STATUS_REG (27h)

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
-------	-----	-----	-----	-------	-----	-----	-----

ZYXOR	X, Y and Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous one before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y and Z axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

OUT_X_L (28h), OUT_X_H (29)

X-axis acceleration data. The value is expressed as two's complement.

OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis acceleration data. The value is expressed as two's complement.

OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis acceleration data. The value is expressed as two's complement.

INT1_CFG (30h)

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
-----	----	------	------	------	------	------	------

INT1_CFG description

AOI	AND/OR combination of Interrupt events. Default value: 0. (See Table)
6D	6 direction detection function enable. Default value: 0. (See Table)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Interrupt 1 source configurations:

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

INT1_SRC (31h)

0	IA	ZH	ZL	YH	YL	XH	XL
---	----	----	----	----	----	----	----

INT1_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z High event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

INT1_THS (32h)

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0
---	------	------	------	------	------	------	------

INT1_THS description

THS6 - THS0 Interrupt 1 threshold. Default value: 000 0000

INT1_DURATION (33h)

0	D6	D5	D4	D3	D2	D1	D0
---	----	----	----	----	----	----	----

INT2_DURATION description

D6 - D0 Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

INT2_CFG (34h)

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
-----	----	------	------	------	------	------	------

INT2_CFG description

AOI	AND/OR combination of interrupt events. Default value: 0. (See table below)
6D	6 direction detection function enable. Default value: 0. (See table below)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

Configuration register for Interrupt 2 source.

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

INT2_SRC (35h)

0	IA	ZH	ZL	YH	YL	XH	XL
---	----	----	----	----	----	----	----

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X Low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read only register.

Reading at this address clears INT2_SRC IA bit (and the interrupt signal on INT 2 pin) and allows the refreshment of data in the INT2_SRC register if the latched option was chosen.

INT2_THS (36h)

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0
---	------	------	------	------	------	------	------

INT2_THS description

THS6 - THS0 Interrupt 1 threshold. Default value: 000 0000

INT2_DURATION (37h)

0	D6	D5	D4	D3	D2	D1	D0
---	----	----	----	----	----	----	----

INT2_DURATION description

D6 - D0 Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

9.2 Register ITG-3200

This section details each register within the InvenSense ITG-3200 gyroscope. Note that any bit that is not defined should be set to zero in order to be compatible with future InvenSense devices.

The register space allows single-byte reads and writes, as well as burst reads and writes. When performing burst reads or writes, the memory pointer will increment until either reading or writing is terminated by the master, or the memory pointer reaches certain reserved registers between registers 33 and 60.

Who Am I (0h)

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	ID							-

Description:

This register is used to verify the identity of the device.

Parameters:

ID Contains the I2C address of the device, which can also be changed by writing to this register.

The Power-On-Reset value of Bit6: Bit1 is 110 100.

Sample Rate Divider (15h)

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
15	21	SMPLRT_DIV								00h

Description:

This register determines the sample rate of the ITG-3200 gyros. The gyros outputs are sampled internally at either 1kHz or 8kHz, determined by the *DLPF_CFG* setting (see register 22). This sampling is then filtered digitally and delivered into the sensor registers after the number of cycles determined by this register. The sample rate is given by the following formula:

$F_{\text{sample}} = F_{\text{internal}} / (\text{divider} + 1)$, where F_{internal} is either 1kHz or 8kHz

As an example, if the internal sampling is at 1kHz, then setting this register to 7 would give the following:

$F_{\text{sample}} = 1\text{kHz} / (7 + 1) = 125\text{Hz}$, or 8ms per sample

Parameters:

SMPLRT_DIV Sample rate divider: 0 to 255

DLPF, Full Scale (16h)

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
16	22	-			FS_SEL		DLPF_CFG			00h

Description:

This register configures several parameters related to the sensor acquisition.

The *FS_SEL* parameter allows setting the full-scale range of the gyro sensors, as described in the table below. The power-on-reset value of *FS_SEL* is 00h. **Set to 03h for proper operation.**

FS_SEL

FS_SEL	Gyro Full-Scale Range
0	Reserved
1	Reserved
2	Reserved
3	$\pm 2000^\circ/\text{sec}$

The *DLPF_CFG* parameter sets the digital low pass filter configuration. It also determines the internal sampling rate used by the device as shown in the table below.

DLPF_CFG

DLPF_CFG	Low Pass Filter Bandwidth	Internal Sample Rate
0	256Hz	8kHz
1	188Hz	1kHz
2	98Hz	1kHz
3	42Hz	1kHz
4	20Hz	1kHz
5	10Hz	1kHz
6	5Hz	1kHz
7	Reserved	Reserved

Parameters:

FS_SEL Full scale selection for gyro sensor data

DLPF_CFG Digital low pass filter configuration and internal sampling rate configuration

Interrupt Configuration (17h)

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
17	23	ACTL	OPEN	LATCH_INT_EN	INT_ANYRD_2CLEAR	0	ITG_RDY_EN	0	RAW_RDY_EN	00h

Description:

This register configures the interrupt operation of the device. The interrupt output pin (INT) configuration can be set, the interrupt latching/clearing method can be set, and the triggers for the interrupt can be set. Note that if the application requires reading every sample of data from the ITG-3200 part, it is best to enable the raw data ready interrupt (*RAW_RDY_EN*). This allows the application to know when new sample data is available.

Parameters:

ACTL Logic level for INT output pin – 1=active low, 0=active high

OPEN Drive type for INT output pin – 1=open drain, 0=push-pull

LATCH_INT_EN Latch mode – 1=latch until interrupt is cleared, 0=50us pulse

INT_ANYRD_2CLEAR Latch clear method – 1=any register read, 0=status register read only

ITG_RDY_EN Enable interrupt when device is ready (PLL ready after changing clock source)

RAW_RDY_EN Enable interrupt when data is available

0 Load zeros into Bits 1 and 3 of the Interrupt Configuration register.

Interrupt Status (1Ah)

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
1A	26	-	-	-	-	-	ITG_RDY	-	RAW_DATA_RDY	00h

Description:

This register is used to determine the status of the ITG-3200 interrupts. Whenever one of the interrupt sources is triggered, the corresponding bit will be set. The polarity of the interrupt pin (active high/low) and the latch type (pulse or latch) has no affect on these status bits.

Use the Interrupt Configuration register (23) to enable the interrupt triggers. If the interrupt is not enabled, the associated status bit will not get set.

In normal use, the *RAW_DATA_RDY* interrupt is used to determine when new sensor data is available in either the sensor registers (27 to 32). Interrupt Status bits get cleared as determined by *INT_ANYRD_2CLEAR* in the interrupt configuration register (23).

Parameters:

ITG_RDY PLL ready

RAW_DATA_RDY Raw data is ready

Sensor Registers (1Bh to 22h)

Type: Read only

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1B	27	TEMP_OUT_H							
1C	28	TEMP_OUT_L							
1D	29	GYRO_XOUT_H							
1E	30	GYRO_XOUT_L							
1F	31	GYRO_YOUT_H							
20	32	GYRO_YOUT_L							
21	33	GYRO_ZOUT_H							
22	34	GYRO_ZOUT_L							

Description:

These registers contain the gyro and temperature sensor data for the ITG-3200 parts. At any time, these values can be read from the device; however it is best to use the interrupt function to determine when new data is available.

Parameters:

TEMP_OUT_H/L 16-bit temperature data (2's complement format)

GYRO_XOUT_H/L 16-bit X gyro output data (2's complement format)

GYRO_YOUT_H/L 16-bit Y gyro output data (2's complement format)

GYRO_ZOUT_H/L 16-bit Z gyro output data (2's complement format)

Power Management (3Eh)

Type: Read/Write

Register (Hex)	Register (Decimal)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
3E	62	H_RES ET	SLEEP	STBY _XG	STBY _YG	STBY _ZG	CLK_SEL			00h

Description:

This register is used to manage the power control, select the clock source, and to issue a master reset to the device.

Setting the *SLEEP* bit in the register puts the device into very low power sleep mode. In this mode, only the serial interface and internal registers remain active, allowing for a very low standby current. Clearing this bit puts the device back into normal mode. To save power, the individual standby selections for each of the gyros should be used if any gyro axis is not used by the application.

The *CLK_SEL* setting determines the device clock source as follows:

CLK_SEL:

CLK_SEL	Clock Source
0	Internal oscillator
1	PLL with X Gyro reference
2	PLL with Y Gyro reference
3	PLL with Z Gyro reference
4	PLL with external 32.768kHz reference
5	PLL with external 19.2MHz reference
6	Reserved
7	Reserved

On power up, the ITG-3200 defaults to the internal oscillator. It is highly recommended that the device is configured to use one of the gyros (or an external clock) as the clock reference, due to the improved stability.

Parameters:

H_RESET Reset device and internal registers to the power-up-default settings

SLEEP Enable low power sleep mode

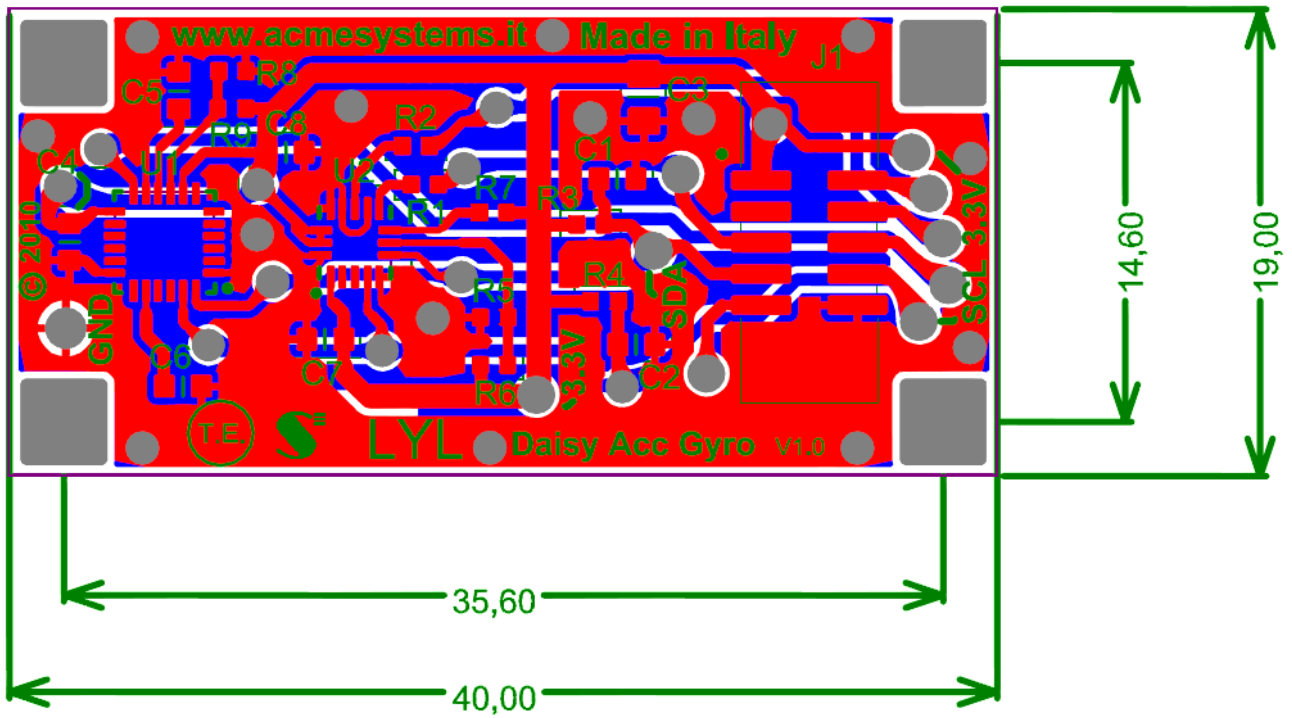
STBY_XG Put gyro X in standby mode (1=standby, 0=normal)

STBY_YG Put gyro Y in standby mode (1=standby, 0=normal)

STBY_ZG Put gyro Z in standby mode (1=standby, 0=normal)

CLK_SEL Select device clock source

10.0 Package information



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